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ATTORNEY NO.: 1690
 CLIENT/MATTER NO.: 27324-0006
 DATE: June 24, 2003

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Enclosed is the Information Disclosure Statement you requested for application number 09/530,553.

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UNDER THE PATENT COOPERATION TREATY-CHAPTER II

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INFORMATION DISCLOSURE STATEMENT
ACCOMPANYING THE FILING OF AN APPLICATION

APPLICANT(S): Gerald Deboy et al.
ATTORNEY DOCKET NO.: P00,0578
INTERNATIONAL APPLICATION NO.: PCT/DE98/03197
10 INTERNATIONAL FILING DATE: 02 November 1998
INVENTION: "HIGH VOLTAGE RESISTANT EDGE STRUCTURE FOR
SEMICONDUCTOR COMPONENTS"

Assistant Commissioner for Patents
Washington, D.C. 20231

15 S I R:

In accordance with the provisions of 37 C.F.R. § 1.56, Applicants request that
citation and examination of the following references be made during the course of
examination of the above-referenced application for United States Letters Patent.

I. SUBMITTED REFERENCES

20 AA United States Patent No. 4,750,028
AB United States Patent No. 4,573,066
AC United States Patent No. 4,633,292
AD United States Patent No. 3,405,329
AE United States Patent No. 4,468,686
25 AL Japanese Patent No. 02-142184
AM German Patent Application No. 196 04 043
AN Japanese Patent No. 08-078661
AO German Patent Application No. 44 10 354
AP Japanese Patent No. 01-272152
30 AQ Canadian Patent No. 667,423

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AR M. Nagata et al., "A Planar 2500V 0.3A Bipolar Transistor for High Voltage Control Circuit", Proc. of 1992 International Symposium on Power Semiconductor Devices and ICs, Tokyo, May 19, 1992, pp. 333-338.

II. EXPLANATION OF RELEVANCE

5 References AA, AB, AC, AL, AM, AN, AO, AP and AR were cited during earlier PCT examination proceedings. Reference AL, which is in Japanese, discloses a semiconductor device and manufacture thereof. Reference AM, which is in German, discloses vertical MOS field effect transistor device. Reference AN, which is in Japanese, discloses a semiconductor element for power. Reference AO, which is in German, discloses a planar structure power semiconductor element for electric drive circuit. Reference AP, which is in Japanese, discloses a semiconductor element with guard ring. Since References AA, AB, AC and AR are in English, no further commentary concerning their teachings is necessary.

15 References AD, AE and AQ were cited for the reasons noted in the Applicants' specification. Since References AD, AE and AQ are in English, no further commentary concerning their teachings is necessary.

 None of the above references discloses or suggests a high voltage resistant edge structure for semiconductor components as disclosed in the present invention.

20 Copies of each of the above references together with Form 1449 are submitted herewith in accordance with 37 C.F.R. §1.98. Except as provided, the undersigned does not possess English translations of the non-English references.

 This Information Disclosure Statement is being submitted simultaneously with the filing of the present application, and is therefore in compliance with 37 C.F.R. §1.97(b) and no fee is necessary.

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All claims of the application are patentable over the teachings of the above references, taken singly or in combination. Early consideration of the application is therefore respectfully requested.

Submitted by,

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(Reg. 31,870)

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